Communications Over Power Lines

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ABSTRACT

The Electrical Industries Association has nearly completed the IS-60 Home Automation Standard which will allow the integration of every appliance in the home. This standard is known as the Consumer Electronic Bus and two versions of the standard have been published - one in 1989 and another in 1992. The standard covers six possible media for communication between devices, the most important at this stage being the power line which allows retrofitting into existing buildings.

This standard is summarised with focus on the PLBus (Power Line Bus). An implementation of the standard's communication technique, comprising of both hardware and software, is outlined and analysed. All components of this system are described and analysed to demonstrate that they perform to the specifications set in the standard.

1. INTRODUCTION

Science fiction writers described technology based houses many decades ago. Asimov for instance writes of a robot running the house - ensuring the climate is to the owners satisfaction and the music suits their mood, as well as answering the door and phone. These technologies are in the very early stages of development, but the technology is now available to make life at home much more simple and enjoyable, saving money as a bonus. This new technology may even be more effective than the aforementioned robots.

Most home appliances have built in microprocessors and are 'smart' in their own way, but true independence for any owner from the chores of modern day living will only be achieved when appliances are part of one intelligent system. In 1984 the Electrical Industries Association (EIA) formed the CEBus (Consumer Electronic Bus) Committee to produce a standard for communication between all devices in the home. This standard, known as EIA IS-60 Home Automation Standard, is nearing completion with the second version [1] being published in 1992. The standard aims for the capability of working with any appliance and to enable retrofitting into an existing home. It is modelled on four of the seven ISO's OSI layers on a network comprising of six possible media. One of these media is the power line which allows a system to be installed in existing residences without modifications to the building. The idea of 'plug and play' is central to the standard. A 'black box' between the appliance and the wall socket enables the appliance to communicate with other devices over the power line.

In the near future, by the turn of the century, we could well find ourselves living in homes that manage themselves using this standard. The stereo would start playing as soon as we walk through the front door, and would turn itself down whenever the doorbell or phone rings. Lights left on in rooms that had been unattended for more than ten minutes would switch themselves off. In winter the heaters would switch on twenty minutes before we were due home. When we go away, the system would randomly turn appliances on and off to give the appearance of occupancy. Our energy bills would be drastically reduced due to more efficient management of appliances to use off peak times if possible.

It is the aim of this paper to implement the CEBus standard for the power line media - also known as the PLBus (Power Line Bus). The focus of the design is on the encoding and modulating functions of the Physical Layer, although the higher layers are implemented in a simplistic form to provide interaction between the Physical Layer and the outside world. The implementation covers both hardware and software which are presented separately as subsystems of the whole. Prior to this is a general overview of the theory of the CEBus standard.

2. CONSUMER ELECTRONIC BUS

2.1 Layers

In 1983, the International Standards Organisation (ISO) completed the Open Systems Interconnection (OSI) network model. The model splits network communication into seven components each performed by a different layer as shown in Figure 1. Three of the layers are of little use in the specific application of the CEBus. The Transport Layer, which provides flow control and error control, is omitted but some of its functions are implemented in the Network and Application Layers. The Session Layer, which specifies how a specific interaction is set up between user and computer, and the Presentation Layer, which provides services that allow the user to interpret the meaning of the information being transferred between different systems, are both unnecessary complications for the network of the CEBus, and are therefore omitted. Reducing the number of layers also reduces the packet length which in turn reduces the loading on the network.

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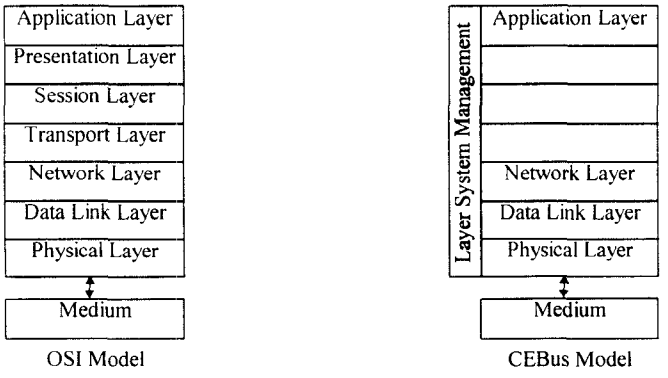

Figure 1 Comparison of the OSI and CEBus Layers

The Application Layer is responsible for interfacing with the user (human or appliance) and interpreting between the CAL (common application language) messages and I/O from the physical world. The Network Layer provides the switching and routing functions to establish, maintain, and terminate connections for data transfer between nodes. The Data Link Layer provides the Network Layer with an apparently error free communication channel by implementing frame assembly and disassembly, error detection and flow control. These functions are performed by two sublayers: the LLC (Logical Link Control) layer provides information about the mode of transmission, while the MAC (Medium Access Control) layer completes the packet for transmission, monitors the addresses for its own incoming packets, and performs error detection using a checksum.

Each node is physically connected to the communications medium through the Physical Layer, also consisting of two sublayers, which is dependant upon the medium to which it is attached. The SE (Symbol Encoding) layer converts the CEBus symbols of the MPDU (MAC protocol data unit) received from the MAC layer into electrical transmission signals. The MDP (Medium Dependant Physical) layer performs the actual modulation of the signal such that it may be placed on the line. Each layer provides acknowledged and unacknowledged connectionless [2] services to the above layer.

The CEBus standard specifies six media for the communication between nodes: Power Line, Twisted Pair, Radio Frequency, Infra Red, Optical Fibre, and Coaxial Cable. The characteristics of the medium determine the frequency, encoding and modulation techniques used. This document is particularly concerned with the Power Line medium.

2.2 Communications

Each medium has a carrier signal which is designed according to the properties of the media. The signal for the Power Line medium specified in the 1992 version of the standard is a sweeping 'chirp' waveform, chosen for its noise immunity properties. For simplicity, the 120kHz sine wave of the 1989 standard is used in this implementation [3].

The CEBus modulation scheme is Non Return to Zero - Pulse Width Encoding (NRZ-PWE). The communication medium can be in one of two states: SUPERIOR - the presence of a signal on the medium; or INFERIOR - the absence of a signal. A SUPERIOR state will always override an INFERIOR state. A unit symbol time (UST) is defined for each medium as the shortest pulse in the encoding scheme. Four symbols are defined by the length of the pulse (as an integral multiple of USTs) and are independent of the state as shown in Figure 2. That is, the same symbol is represented by a 1UST SUPERIOR pulse and a 1UST INFERIOR pulse. The binary values '1' and '0', converted to symbols ONE and ZERO, are represented by a 1UST and 2UST pulse respectively. Each field in a packet is separated by a end of field symbol (EOF) represented by a 3UST pulse and the end of the packet is announced with an EOP symbol represented by a 4UST pulse.

On the Power Line medium, the carrier signal is a 120kHz sine wave. The line is SUPERIOR when the 120kHz signal is present, and INFERIOR otherwise.

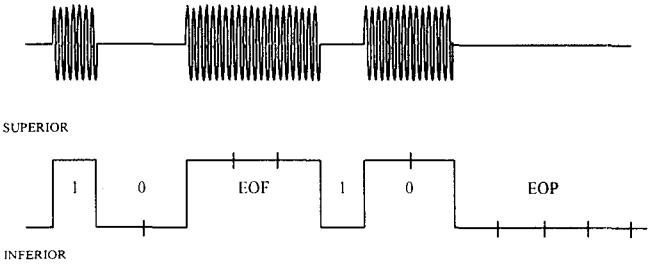

Figure 2 CEBus Modulation Technique

Messages are transmitted between nodes in the form of an MPDU or 'packet' made up of fields as outlined below:

Preamble - a pseudo-random 8 bit field used for contention purposes.

Control Field - generated by the Data Link Layer to pass information about the contents of the packet.

Destination Address - specifies the 'name' of the node the packet is directed to. The address may correspond to a unique device, a group of devices, or all devices. If the packet is to be broadcast to all devices, the field is left blank.

Destination House Code - specifies the residence 'name' from a group of residences connected to the same media (in this case - to the same power line distribution transformer).

Source Address - specifies the 'name' of the device transmitting the packet. The field is optional and may be left blank.

Source House Code -specifies the 'name' of the residence to which the transmitting device belongs. If this field is blank, while the Source Address field is not, the Source House Code is assumed to be the same as the Destination House Code.

Information Field - The information field (sometimes referred to as the Data Field) is up to 32 bytes long, subject to leading zero suppression (see section 2.3). It contains

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the CAL command that the system is designed to pass. In cases where the packet is solely for acknowledgment, the field may be empty.

Checksum Field - The CEBus uses a 16 bit Cyclic Redundancy Check (CRC) for the PLBus or an 8-bit checksum for all other media (see section 2.4) to detect errors.

2.3 Leading Zero Suppression

Leading zeros, defined in the standard as "zeros more significant than the most significant one", don't effect the values of the binary number to which they belong. They may therefore be removed, reducing the packet length. Thus the length of each field becomes variable, and the individual fields are distinguishable by the EOF separators. Figure 3 shows how a given field would be transmitted.

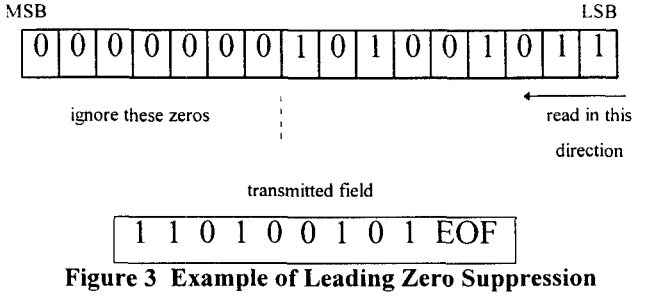

Figure 3 Example of Leading Zero Suppression

2.4 Error Detection

It is desirable to ignore any packets which have been damaged by noise on the line. Such packets are recognised through the use of the checksum field. The 1992 standard recommends the widely used CRC-16 for the Power Line medium, but insufficient memory prevents us from implementing it in software. At this early stage of the development, therefore, the alternative 8-bit checksum recommended for all other media is used.

The checksum is a simple form of error detection, albeit not very reliable. It relies upon the sum of all bytes in the packet, excluding the corruptible Preamble, equalling zero (ignoring carries). The value for the checksum is found as shown in Figure 4. All the relevant bytes are added and the 2's complement of the resulting sum is taken as the checksum. The 2's complement is calculated by taking the 1's complement (exclusive OR with $FF) and adding 1.

This form of checksum is not as effective in detecting errors as the CRC, but is effective for current testing purposes.

3. HARDWARE

3.1 Overview

Below, Figure 5, is a block diagram of the individual hardware subsystems and their relation to each other. Each of the components are explained in the following sections. All layers higher than the MDP layer are implemented in software

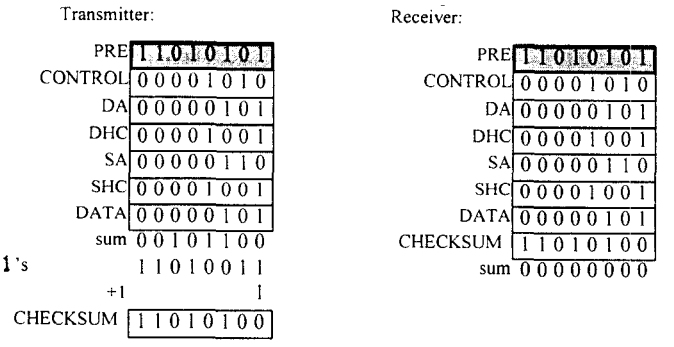

Figure 4 Calculating and Checking the Checksum

using the MC68HC811E2 microprocessor as outlined in chaper 4.

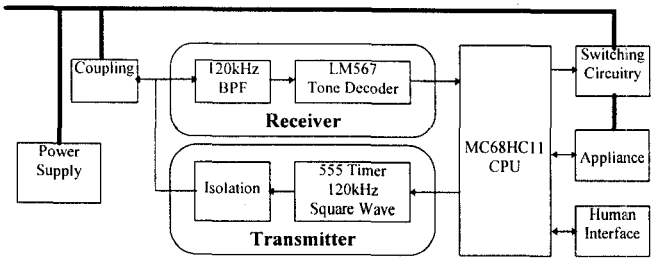

Figure 5 The Complete System

3.2 Transmitter

The signal is generated by the MC68HC11 software and output as a TTL logic signal on the Timer Output Compare pin TOC2. This is output in a two level DC format with 5V representing SUPERIOR and common representing INFERIOR. This signal is then used to drive a 555 timer to produce the 120kHz square wave. The 555 timer was chosen because of its low cost, reliability, and drive capability [4]. The resulting circuit is shown in Figure 6. The timing resistors and capacitor have been chosen using the data sheets [4]. A diode is included to remove R_2 from the charge path enabling a 50% duty cycle. The two timing resistors have a variable component to a allow fine tuning.

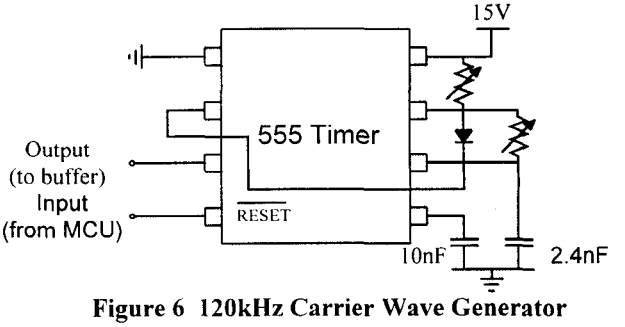

Figure 6 120kHz Carrier Wave Generator

To achieve maximum signal transfer, we wish the input of the receiving circuit (555 is inactive) to be large compared with the output impedance of the transmitting circuit (555 is active). A simple emitter-follower amplifier circuit has similar properties if R_E is large [5] as in Figure 7. This circuit

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also serves as protection for the 555 against negative voltages coming from the line.

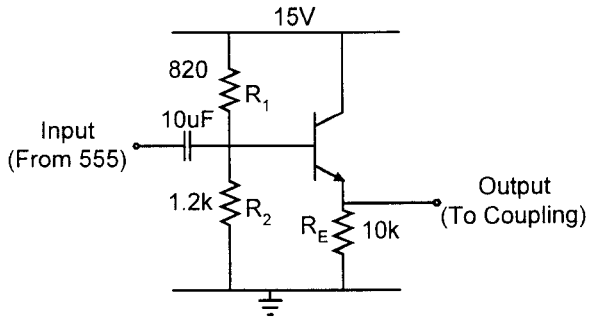

Figure 7 Emitter-Follower Transistor Isolation

The output wave is still in the form of a square wave. The high order harmonics are filtered using the coupling circuit of section 3.4. The wave resulting on the line is the fundamental 120kHz with DC removed.

3.3 Receiver

The signal received from the external nodes is already filtered of 50Hz by the mains coupling, but both internal (the nodes own transmitter) and external (input from the line) signals need to be filtered for high frequency noise, and the internally generated signal of its DC component. To this end, we use a 2nd order band pass filter centred on 120kHz. The design is the same as that used for the mains coupling, see section 3.4, but the capacitors need not be rated for high voltage.

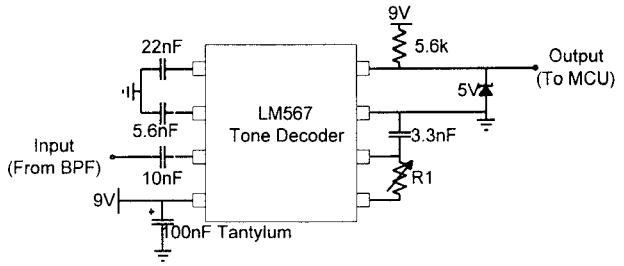

Figure 8 120kHz Tone Decoder

The microprocessor needs the incoming packet in a form similar to that transmitted by the responsible microprocessor. The TTL logic levels are obtained by demodulating the incoming 120kHz sine wave. An appropriate, and simple solution was found in the LM567 tone decoder [4]. This chip consists of a phase lock loop and a voltage controlled oscillator which can be adjusted though external components. The resulting circuit taken from the data sheets is shown in Figure 8. C_1 is set at 33nF and R_1 at 230Ω, found using the data sheets to set the centre frequency at 120kHz. with a variable component for fine tuning. C_2 is chosen as 5.6nF to give a bandwidth of 20kHz. If we choose V_{CC} to be 9V, the tone decoder will accept inputs between -10V and 9.5V so the 555 output (approximately 0V to 15V) need only be filtered for DC. The output is 0V when the signal is present and V_{CC}=9V when absent, so clipping is needed before the signal is passed to the TTL pins on the MCU. A zener diode with a reverse breakdown voltage of 5V is used to perform the clipping. No inversion of the signal is necessary since the receiver software detects edges not states.

3.4 Mains Coupling

Most of the components used in the circuitry surrounding the MC68HC11 are incapable of handling more than 10-15 volts. The aim of this project, however, is to transmit signals determined by the circuitry over 240V mains power lines. It is therefore essential to have some means of connecting the system to the mains while removing the large voltages. This is the role of mains coupling.

A series capacitor - inductor circuit is used to act as a band pass filter as shown in Figure 9. The 50Hz mains signal is over three decades lower than the 120kHz frequency used to signal. Consequently, there is over 60dB attenuation on the 50Hz wave which reduces it from 240V to below 0.3V, a voltage that will not interfere with the system. The capacitor must be capable of withstanding high voltages (600V) so as to ensure no arcing which may destroy the system. Two separate high voltage capacitors are used as an extra safety precaution - if one is faulty or breaks down, the other will safely isolate the system. Losing one of the capacitors to arcing will not have a substantial effect on the filtering properties of the coupling which will still have over 50dB attenuation at 50Hz.

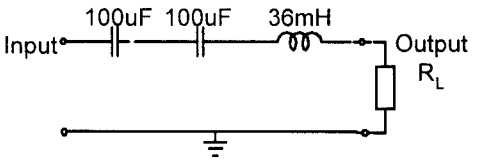

Figure 9 Coupling Circuit

3.5 Switching Circuitry

In many cases, the microprocessor in this system will be used to switch a load. Assuming the load controlled by the system is powered by 240V, we will need a relay to switch it. Classical relays may be excessively noisy (to the human ear) as well as bulky, so it was decided that a triac would be more suitable for the purposes of a home system. The MOC3021 Opto Triac Driver is a 100mA triac driven by a 1.1V LED. While this is ideal for any 24W load

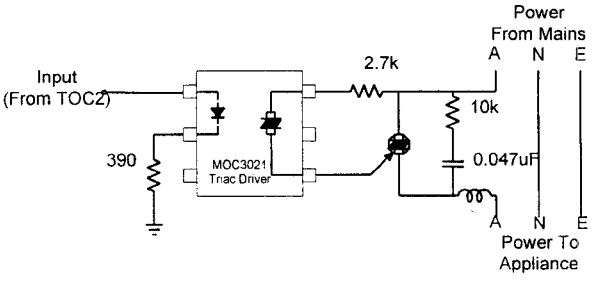

Figure 10 Triac Switching Circuitry

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($P = VI = 240Vrms \times 100mA = 24W$), most appliances have a higher power rating and a larger triac is needed. Here, a 10A triac is used, since it doesn't take any extra space, and is capable of driving any standard mains appliance. For specific appliances, this triac may be changed without effecting the circuit. The circuit used is shown in Figure 10.

3.6 Microprocessor

The MC68HC811E2 [6], shown in Figure 11 is equipped with 2Kbytes of Electrically Erasable Programmable Read Only Memory (EEPROM) which enables the chip to be reprogrammed whenever a new appliance is added to the system. The MCU's (microcontroller unit) clock is run by an external crystal oscillator. For this application we have chosen an 8MHz crystal, wired as in 2-9,11 on page 2-13 of the manual [6]. This provides a clocking rate of 2MHz enabling exactly 2000 cycles per UST. It also allows serial communication at 300, 1200, 2400, 4800, and 9600 baud. This will enable communication with a PC to be implemented with minimal effort. The 16 bit counter, resident on the MCU, is one of the standard registers and is therefore readily accessible to the software. It has a range of 2^{16}=65536, which at 2MHz spans 32.768ms. This is sufficient to cope with the largest pulse which spans 4ms.

There are five separate ports on the MCU, each of which has its own special functions. These ports, their functions, and their applications in this paper are outlined below. The pins of each of these ports are pulled up to the 5V supply with 100kΩ resistors to minimise loss in the CMOS circuits through floating. Each of the pins can source or supply up to 25mA safely which is enough to run all attached hardware.

PORT A - Port A provides the most useful aspect of this MCU for the CEBus system. It has direct access to the counter, and each individual pin with its own 16 bit register is able to provide interrupts. Five of the pins are Timer Output Compare (TOC) pins are the basis of the transmission algorithm. When enabled, they will cause an interrupt when the corresponding register holds the same value as the counter. Each pin can be enabled individually to be set high, low, remain unchanged, or toggle on a match with the counter, or to ignore it completely (no interrupt). The remaining three pins are Timer Input Capture (TIC) pins which are used to inform the CPU (central processing unit) of an incoming signal. Each pin can be individually enabled, and set to interrupt on either a rising edge, a falling edge, or both and will record the time (counter value) at which the edge occurred.

PORT B - Port B is an output port with handshake. It is used for general outputs such as human or appliance interfacing, and was invaluable in the design process for debugging.

PORT C - Port C is a handshaking bidirectional I/O port. It is used to poll the keypad for input.

PORT D - Port D provides both synchronous and asynchronous communication. This will be useful for communicating with a PC.

PORT E - Port E is an input port with the option of analogue to digital conversion. At this stage we will only be controlling digital appliances, but future developments such as monitoring temperature might possibly require the converter. It is currently used to set the node's address by attaching a DIP switch array.

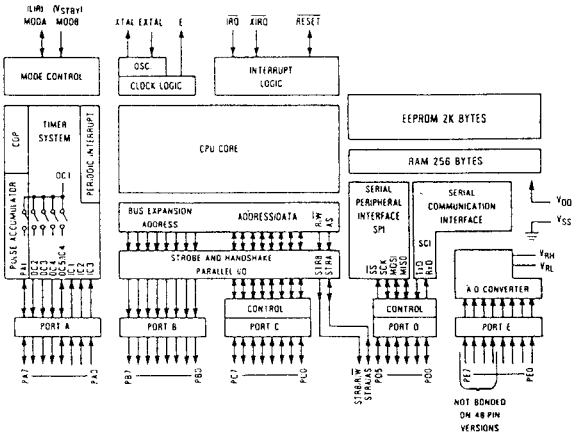

Figure 11 The MC68HC811E2 Microprocessor

4. SOFTWARE

Software is used to implement the layers higher than, and including the Symbol Encoding layer. Most emphasis is placed on the SE layer with a skeleton implementation of higher layers to provide interfacing between the Physical Layer and the user or appliance.

4.1 Layer System Management

The Layer System Management is the main loop of the program. It coordinates all the layers of the protocol by calling on them when their respective parameters are ready for processing. Since it is not necessary to be able to both transmit and receive simultaneously, the form of the Layer System Management would be as shown in Figure 12.

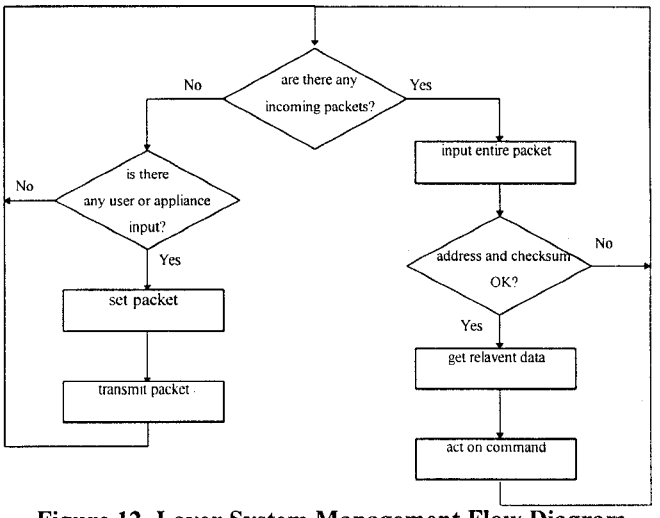

Figure 12 Layer System Management Flow Diagram

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4.2 Application Layer

The transmit component of the Application Layer polls the keypad on port C to test for new input. If there is an input, it stores it and passes it to the lower layers.

When the Application Layer receives a packet from the lower layers, the data frame is read, and the value decoded and acted upon accordingly.

4.3 Data Link Layer

Before transmitting, the packet is constructed and passed to the lower layers. The Source Address field is taken from the DIP switches on port E, the input passed down from the Application Layer is inserted directly into the Information field, and the checksum is calculated as described in section 2.4. The rest of the packet is hard coded since those fields are not used explicitly.

This component of the receive procedure checks if the packet is addressed to this node, by comparison with the DIP switches on port E, and that there are no errors. The packet is checked for errors by summing all fields, excluding the preamble, and comparing the result to zero as in section 2.4.

4.4 Symbol Encoding Layer

This layer converts between the software packet and a series of digital pulses as described in section 2.2. The resulting procedure for the transmitter follows the flow chart shown in Figure 13.

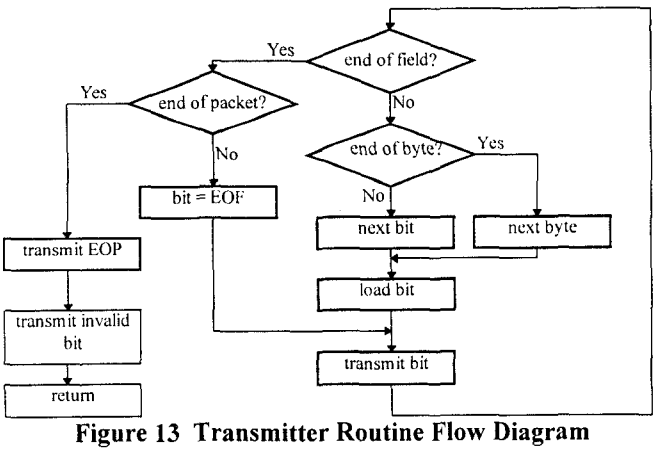

Figure 13 Transmitter Routine Flow Diagram

The bit is transmitted by setting an interrupt to occur on a Timer Output Compare pin at the correct time with a toggle on the state of that pin.

The receiver routine is triggered by the first edge of the incoming packet causing an interrupt on a Timer Input Capture pin. The interrupt routine converts the incoming pulses into symbols and passes them to the main receiver routine. They are them interpreted and inserted into the receiver buffer accordingly. When an EOF is received, the field size is stored and the field pointers are incremented. Upon receiving an EOP, the SE layer passes the complete packet to the MAC layer and exits. The resulting flow chart is shown in Figure 14.

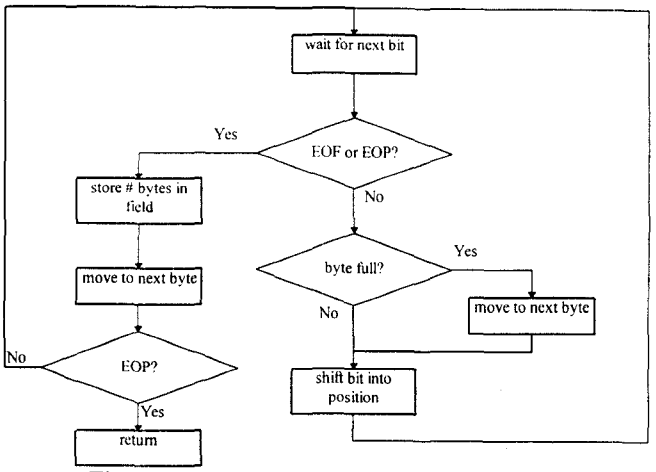

Figure 14 Receiver Routine Flow Diagram

The receiver interrupt routine converts pulses into symbols which it passes back to the main receiver routine. It ignores pulses outside the acceptable range (±0.5UST) as errors. The lengths of the bits are determined by recording the times at which the edges occur and taking the difference as the pulse length. For the purpose of removing glitches in this implementation, the routine sleeps for 100μs before testing the line. If it has reverted, it is assumed the detected edge was the first edge of a glitch.

4.5 Leading Zero Suppression

Both the transmitted and received packets are stored in dual buffers. The first is fixed at eight bytes and holds the size, in bytes, of each of the eight fields of the packet. The second variable length buffer holds the packet itself. This minimises the memory needed for the storage of the packet while allowing leading zero suppression and ease of use by the SE layer. The transmit buffer is shown in Figure 15 and the receive buffer is of a similar format. Each routine keeps track of its current position in each of the buffers using index registers.

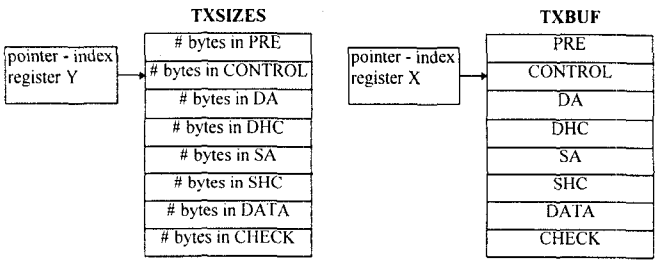

Figure 15 Transmit Buffer Implementation

When transmitting, the SE layer loads the number of bytes in the current field then decrements that count whenever it loads a new byte. It transmits all but the last byte by shifting the byte right eight times, transmitting the least significant bit each time. When it reaches the last byte, it uses leading zero suppression to decide when to transmit the EOF

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and skip to the next field. On transmitting every bit the resulting byte is checked. When the byte value is zero, the EOF (or EOP) is transmitted.

The receiver operates by shifting every bit that arrives to its correct position in the byte - least significant bit first. When the byte is full, the pointer moves to the next byte and starts filling from the least significant bit. The routine keeps count of the number of bytes in the current field and stores it upon receiving an EOF or EOP.

5. ANALYSIS

All subsystems were tested for accuracy, with the results outlined below.

The pulse lengths are accurate to 0.1% satisfying the 1% limit specified by the standard. The coupling provides 79dB attenuation at 50Hz, reducing the 240V to below 5mV, and is centred on 120.00kHz with no attenuation. When transmitted over the power line, the 15V signal produced by the 555 timer is received as 12V at the tone decoder.

Figure 16 shows the modulation of a string of EOP symbols. The top waveform is the modulating signal, while the bottom is the modulated signal. This is the signal specified by the standard as presented in Figure 2. The resulting sine wave is at exactly 120kHz frequency. The signal coming off the line at the receiver is shown in the top of Figure 17. This signal when demodulated by the tone decoder is shown at the bottom of Figure 17. Both the original modulating signal and the demodulated signal are displayed together in Figure 18 and Figure 19 with the transmitted signal above and received signal below. Figure 18 shows a string of EOFs, while Figure 19 shows the packet as assembled in 2.4 ERROR DETECTION. The former shows a slight delay of the order of 200μs when reverting to the inferior state due to decay in the signal. This is compensated for by the fact that the software will allow a 0.5UST error in the signal in accordance with the standard. The latter demonstrates that the distortion at the receiver is minimal even over an entire packet. It also shows that the leading zero suppression and checksum algorithms function as designed.

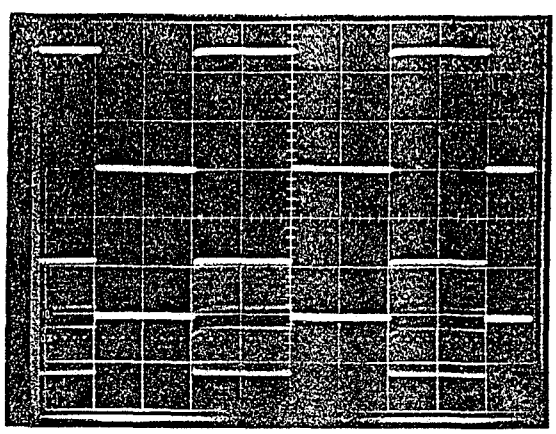

Figure 16 Modulation of a String of EOPs

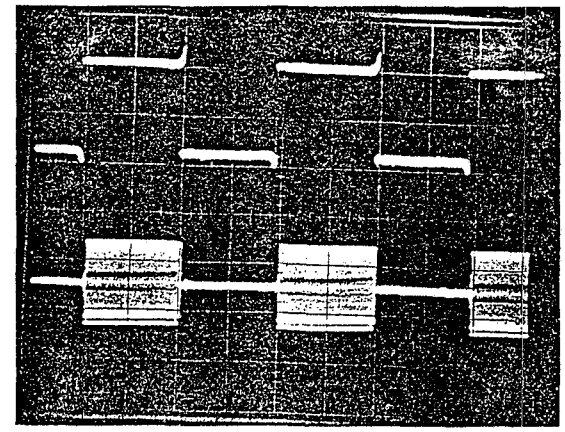

Figure 17 Demodulation of a String of EOPs

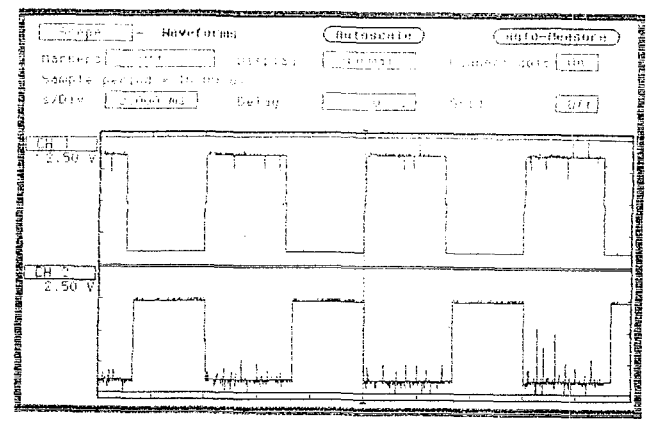

Figure 18 Transmitted and Received Signals

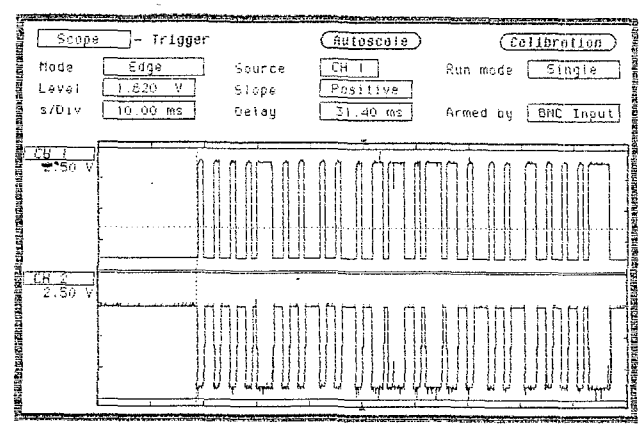

Figure 19 Transmitted and Received Packets

6. CONCLUSION

The work presented in this paper is consistent with the objective of implementing the Power Line Bus. The relevant documentation, including EIA's Home Automation Standard itself, has been researched and summarised. The practical deign included both hardware and software. The implementation covered the complete protocol from the user input through the communication scheme to the control of appropriate appliances.

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At the Application Layer, the microprocessor successfully collects input from a user and passes the data to the lower layers. Upon receiving the data from lower layers, the Application Layer interprets the data and responds correctly by switching the specified appliance. The Network Layer is hard coded for simplicity as is the Logical Link Control layer. The Control field however, does match the standard's specifications for a data carrying packet of standard priority on the power line medium. While all the addresses and the Preamble are hard coded to avoid unnecessary complications, the packet is assembled in the Medium Access Control layer as required by the protocol. The Information field is taken directly from the Application Layer and the Checksum is calculated according to the standard. At the receiver, the packet is disassembled and ignored if the address or Checksum are incorrect.

The Symbol Encoding layer converts the packet to the correct series of pulses for transmission and converts those pulses back to the correct fields at the receiver. Leading zero suppression is implemented, and this layer will also respond correctly to fields of any length. The Medium Dependant Physical layer is implemented completely in hardware. It modulates and demodulates the signal from the SE layer to the form specified by the 1989 standard for the power line. It also performs the buffering, filtering and coupling necessary to make the subsystem become a whole, with safe access to the power line.

All components of the system have been tested individually and as a whole and have been found to perform as expected. The state of the university power supply is such that high frequency signals are filtered out and is unsuitable for the modulation techniques used. This modulation scheme, however, has been tested on an isolated supply and found to perform satisfactorily. It is believed that this implementation will work, as designed, on a residential power circuit.

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